IN THE SPECIFICATION

Please replace the paragraph at page 14, prenumbered line 21, to page 15, prenumbered line 3, with the following rewritten paragraph:

Fig. 4 is a diagram for explaining the operation fault of the gain switching circuit in terms of the input/output characteristics of the preamp. In Fig. 4, characteristic 71 is an input/output characteristic when the preamp operates at the intrinsic gain. Characteristic 72 is an input/output characteristic when the preamp operates at the first conversion gain. Likewise, characteristic 73 is an input/output characteristic when the preamp operates at the second conversion gain. A gain switching point A is a point at which gain switching from the intrinsic gain to the first conversion gain is performed when the output signal exceeds the discrimination level V1, and a gain switching point B is the point at which gain switching from the first conversion gain to the second conversion gain is performed when the output signal exceeds the discrimination level V2.

Please replace the paragraph at page 16, prenumbered line 32, to page 17, prenumbered line 16, with the following rewritten paragraph:

Fig. 5 is a block diagram of an arrangement of a preamp gain switching circuit according to a second embodiment of the present invention. With the gain switching circuit 31 shown in Fig. 5, the gain switching circuit 3 of Fig. 1 is provided with a delaying circuit 21 that delays the output of the level holding circuit 19 by one bit or more and the process of judging whether the discrimination level V2 is exceeded is performed in the two stages of the judging circuit 18 and a judging circuit [[20]] 22. Besides these, the arrangement is the same as or equivalent to the arrangement of the gain switching circuit 3 of the first embodiment shown in Fig. 1 and the same symbols are provided to the respective parts. Also, whereas the two gate signals of the first gate signal and the second gate signal are used to perform

discrimination with respect to the discrimination levels V1 and V2 in the first embodiment, the present embodiment differs in that a single gate signal is used to perform discrimination.

Please replace the paragraph at page 24, prenumbered line 24, to page 25, prenumbered line 1, with the following rewritten paragraph:

Fig. 10 is a block diagram of an arrangement of a gate generating circuit 35 according to a fourth embodiment of the present invention. The gate generating circuit 35 of the fourth embodiment shown in Fig. 10 is another arrangement example of the gate generating circuit 23 shown in Fig. 8. The gate generating circuit 35 has level detecting circuits 24 and [[25]] 24', a variation-point detecting circuit 28, which is a first variation-point detecting circuit, a variation-point detecting circuit 29, which is a second variation-point detecting circuit, and a logical product (AND) circuit 26.

Please replace the paragraph at page 25, prenumbered lines 2-9, with the following rewritten paragraph:

In Fig. 10, the output (voltage signal) B of the TIA 2 is input into one of the input terminals of each of the level detecting circuits 24 and [[25]] 24'. A discrimination level V10, which is the first discrimination level, is input into the other input terminal of the level detecting circuit 24. A discrimination level V11, which is the second discrimination level, is input into the other input terminal of the level detecting circuit [[25]] 24'.

Please replace the paragraph at page 25, prenumbered lines 10-16, with the following rewritten paragraph:

An output L of the level detecting circuit 24 is input into the variation-point detecting circuit 28. An output M of the level detecting circuit [[25]] 24' is input into the variation-

point detecting circuit 29. The respective outputs of the variation-point detecting circuits 28 and 29 are input into the AND circuit 26. The AND circuit 26 outputs a gate signal (GATE).

Please replace the paragraph at page 25, prenumbered lines 17-25, with the following rewritten paragraph:

Fig. 11 is a timing chart for explaining operations of the gate generating circuit 35 shown in Fig. 10. "A" of Fig. 11 depicts a current waveform that is input into the TIA 2 and here, the same signal train as the first to the third packets shown in Fig. [[11]] 9 is shown. "B" of Fig. 11 depicts a waveform of the output voltage (Vout) B output from the TIA 2 when the respective packet signals of "A" are input, and the discrimination levels (V10, V11, V1, and V2) are indicated on the waveform.

Please replace the paragraph at page 26, prenumbered lines 18-30, with the following rewritten paragraph:

"M" of Fig. 11 is a waveform diagram depicting operations of the level detecting circuit [[25]] 24'. For the first packet, because the discrimination level V11 is not exceeded, output pulses are not generated. Meanwhile, for the second packet, because the discrimination level V11 is exceeded, pulses are generated for the periods in which the discrimination level V11 is exceeded. For the third packet, though the signal exceeds the discrimination level V11, unlike the waveform of "L" that results from the comparison with the discrimination level V10, output pulses are generated for the periods in which the discrimination level V11 is exceeded. At the sixth bit and onward, unlike the waveform of "L", output pulses are not generated.

Please cancel the original Abstract at page 34, lines 1-15 in its entirety, and insert therefor the following replacement Abstract on a separate sheet as follows: